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**Semester: 3rd Semester**

**REG#no=20pwcse1952**

**Lab Report#01**

**DLD Lab**

**Department of Computer System Engineering**

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**Submitted to:**

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**Digital Logic Gates**

**Introduction:**

A Digital Logic Gate is an electronic circuit which makes logical decisions based on the combination of digital signals present on its inputs. A logic gate is an idealized model of computation or physical electronic device implementing a Boolean function, a logical operation performed on one or more binary inputs that produces a single binary output. Depending on the context, the term may refer to an ideal logic gate, one that has for instance zero rise time and unlimited fan-out, or it may refer to a non-ideal physical device.

**Logic Gates:**

**There are seven basic logic gates:**

1. **AND**
2. **OR**
3. **XOR**
4. **NOT**
5. **NAND**
6. **NOR**
7. **XNOR**

**NOT Gate**

**TRUTH TABLE:**

|  |  |
| --- | --- |
| Input | Output |
| 0 | 1 |
| 1 | 0 |

**OR Gate**

**TRUTH TABLE:**

|  |  |  |
| --- | --- | --- |
| input | input | output |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

**AND Gate**

**TRUTH TABLE:**

|  |  |  |
| --- | --- | --- |
| **input** | **input** | **output** |
| **0** | **0** | **0** |
| **0** | **1** | **0** |
| **1** | **0** | **0** |
| **1** | **1** | **1** |

**NAND Gate**

**TRUTH TABLE:**

|  |  |  |
| --- | --- | --- |
| **input** | **input** | **output** |
| **0** | **0** | **1** |
| **0** | **1** | **1** |
| **1** | **0** | **1** |
| **1** | **1** | **0** |

**NOR Gate**

**TRUTH TABLE:**

|  |  |  |
| --- | --- | --- |
| **input** | **input** | **output** |
| **0** | **0** | **1** |
| **0** | **1** | **0** |
| **1** | **0** | **0** |
| **1** | **1** | **0** |

**XOR Gate**

**TRUTH TABLE:**

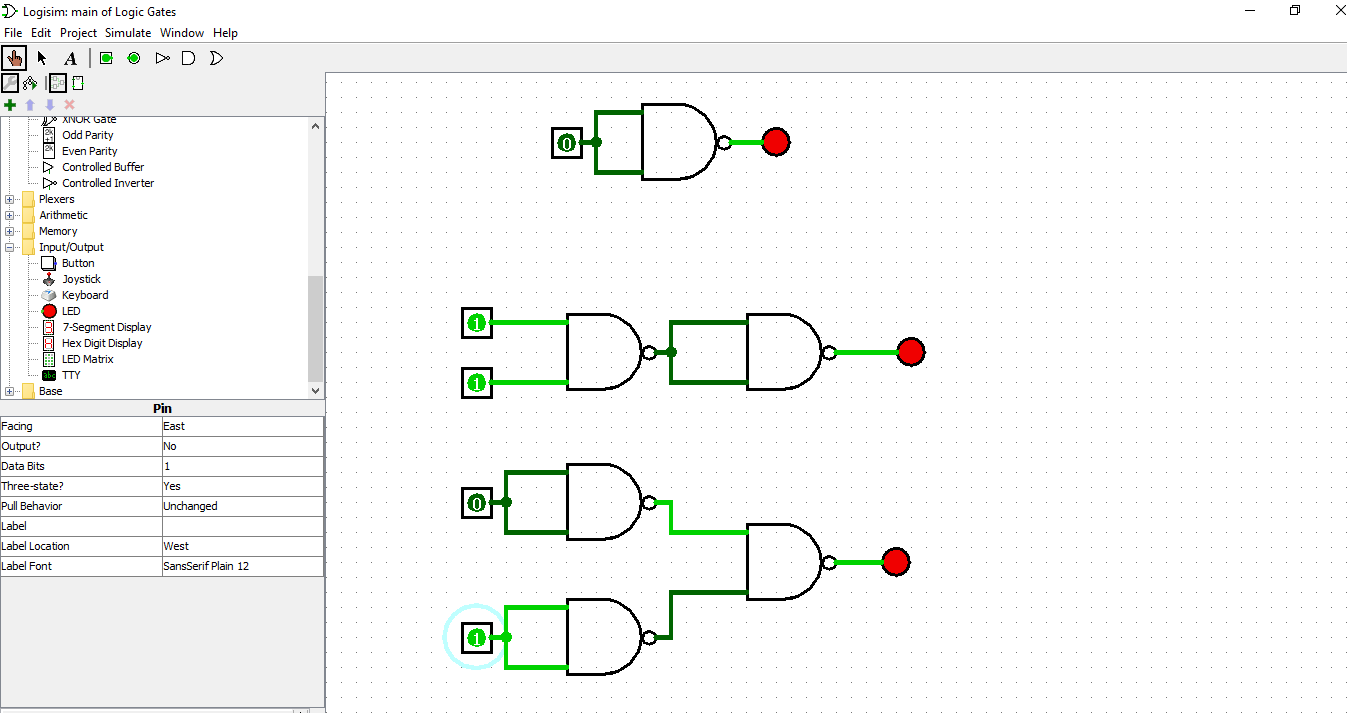
|  |  |  |
| --- | --- | --- |
| **input** | **input** | **output** |
| **0** | **0** | **0** |
| **0** | **1** | **1** |
| **1** | **0** | **1** |
| **1** | **1** | **0** |

**XNOR Gate**

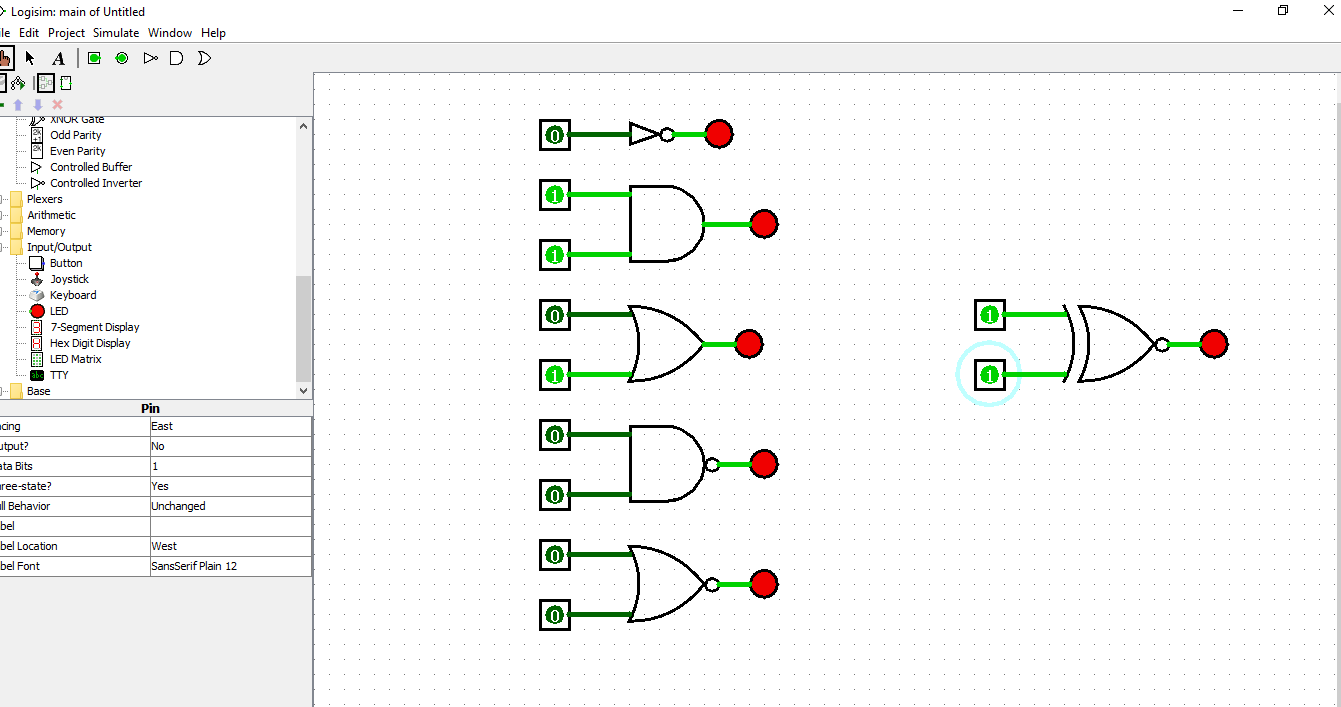
**TRUTH TABLE:**

|  |  |  |
| --- | --- | --- |
| **input** | **input** | **Output** |
| **0** | **0** | **1** |
| **0** | **1** | **0** |
| **1** | **0** | **0** |
| **1** | **1** | **1** |

**Implementing NOT/AND/OR gate using NAND Gates:**

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**Six logic gates are drawen below:**

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